TOPOLOGICAL ANALYSIS OF THYRISTOR CIRCUITS

Babatunde Araoye ADEGBOYE
Department of Electrical Engineering,
Ahmadu Bello University, Zaria.

ABSTRACT
The paper utilises the network topology in the analysis of a thyristor circuit – an oscillating chopper. The graph of the chopper was developed following which the complete incidence matrix was formed. The signal flow graph was also developed, which was reduced directly by the application of Mason's Rule, this being the basis for the formulation of the state equations. For analytical reasons, the diodes and thyristors were classified along with the resistance branches because of their switching properties. The analysis concludes that the problem of varying time constants in the solution of state equations in the thyristor circuits is eliminated by opening the open circuit branches.

KEYWORDS
Chopper, Diode, Graph, Incidence matrix, Node, Signal-flow, State equations, Switching, Thyristor, Topology.

INTRODUCTION

The thyristor has four or more layers and three or more junctions. It has a built-in feature for internal regeneration under special bias conditions, whereby it goes from the off-state (blocking state) to the on-state (conducting state). This property is called "*switching*". Both sides are stable and reversible. It is this property, coupled with its large power-handling capacity, which makes it very useful in power modulation and control. Thyristors belong to the general family of semiconductor devices used for power control [1], the oldest and widely used member being the silicon-controlled rectifier (SCR). It is a four-layer, three-junction device having three terminals, namely, the anode, the cathode and the gate. It is a unilateral device and conduction takes place from anode to cathode under proper bias conditions. The basic thyristor, which is usually designed to possess approximately equal forward and reverse blocking capabilities, exists in two broad classes [2, 3]. The first is the converter grade thyristor, for low frequency use and is designed to have the lowest possible 'on' state voltage drop but will only switch slowly. The second is the inverter grade or fast thyristor designed for higher frequency use and has a fast turn-'off' but generally a higher forward voltage drop than the converter grade device.

Two basic forms of power control are the phase control and the on-off control. In the phase control, the variation in load power at constant input voltage is obtained by changing the firing angle (usually denoted by α in most literature). This form of voltage control is used for d.c. power supplies, temperature regulators, light dimmers and speed regulation of a.c. and d.c. motors. Power control in d.c. circuits is obtained by varying the duration of the on-time and the off-time of the device. Such a mode of operation is called on-off control or chopper control. Voltage is applied for a given period called on-time (T_{ON}) and the load is open-circuited or the applied voltage is removed for a duration known as off-time (T_{OFF}). Control is achieved by varying the on- and off-time. This method is applicable to both a.c. and d.c. circuits. For example, to regulate the speed of a.c. motors, the rms voltage applied to the stator, for a given on- and off-time is given by:

$$V_{rms} = \frac{V_m}{\sqrt{2}} \sqrt{\frac{T_{on}}{T_{on} + T_{OFF}}} \qquad (1)$$

where, V_m is the peak amplitude of the a.c. voltage.
In a.c. circuits with direct on-off control, the load current is alternating and, therefore, a triac can be very conveniently used.

The thyristor circuit considered in this paper is the chopper, which essentially is a d.c. to d.c. converter. The conversion of a fixed voltage source of a d.c. source to a variable, average voltage on a load can be made possible by placing a chopper between the d.c. source and the load [4]. The chopper is a high-speed static switch and finds its application mainly in the d.c. voltage regulator, d.c. motor speed control and battery charging.

PROBLEM DEFINITION

Diodes and thyristors are regarded as switches in digital computations of thyristor circuits [5-7]. The switch is said to be 'on' when it is represented by a series combination of voltage and a small resistance and 'off' when it is represented by a very large resistance. Resistors can represent these switches (either on or off), the values of which depend on the switching state. Since the latter forms a branch of the graph, the evaluation of the associated system equations will result in a widely varying time constants of eigenvalues, a problem that increases the computation time.

Revankar [6] used state equations in analysing a thyristor circuit. His method uses the network topology for the formulation of state equations in a thyristor circuit with the main object of eliminating the problem of widely varying time constants. The present paper uses a purely topological method where the state equations were derived directly from the graph of the chopper.

The actual state variables present for a given set of switching device on/off conditions are decided on the basis of a normal tree constructed from the modified complete incidence matrix. The normal tree is used to formulate the state equations with the main aim of eradicating the problem of widely time varying constants. The construction of the signal-flow graph is, therefore, necessary, which must be reduced to obtain the overall input-output transmittance. The reduced graph eventually provides the desired state equations.

TOPOLOGICAL REPRESENTATION OF THYRISTOR CIRCUITS

Diodes and thyristors are regarded as open circuits when they are 'off'; they are said to have small resistance when they are 'on'. They are, therefore, classified along with the resistance branches. The order in which the network branches are numbered is such that the voltage sources are numbered first, followed by the remaining tree branches (that is, capacitors, resistors, switches and inductors) and finally, the current sources [6, 8]. The branches of the switching devices are oriented from the anode to the cathode in the graph of the thyristor circuit in order to show the possible direction of flow of current. The normal tree is constructed from the modified complete incidence matrix and it is on this basis that the state variables present for a given set of switching device on/off conditions are decided.

COMPLETE INCIDENCE MATRIX

The complete incidence matrix, β_A, is derived if all the branches associated with the graph are present [9]. Next, open circuit branches are removed from the graph in order to eliminate the widely varying time constants. This modified matrix is denoted as β_{AM}.
The removal of the off-switch branches may bring about a node to which only one branch is attached. This is called a hanging node, which also, possibly, brings the hanging branch, which

starts from, or terminates on a hanging node. All hanging nodes and hanging branches observed are removed from the graph.

OPERATION AND TOPOLOGICAL ANALYSIS OF THE CHOPPER

The chopper of Fig. 1 is considered for analysis. The operation is such that the capacitor discharge current passing through it turns off the conducting SCR. L_2 is a large inductor, which makes the load current ripple free. It is assumed that the load current is steady and continuous. Voltage, e, will be equal to supply voltage when SCR_1 is conducting (on-time) and zero when diode D_1 is conducting (off-time). Here, the on-time is fixed by the natural period of the resonant circuit L_1C_1. SCR_1 is triggered by a UJT (unijunction transistor) relaxation oscillator, the frequency determines the (on + off)-time. So this chopper produces a variable-frequency time ratio control (TRC).

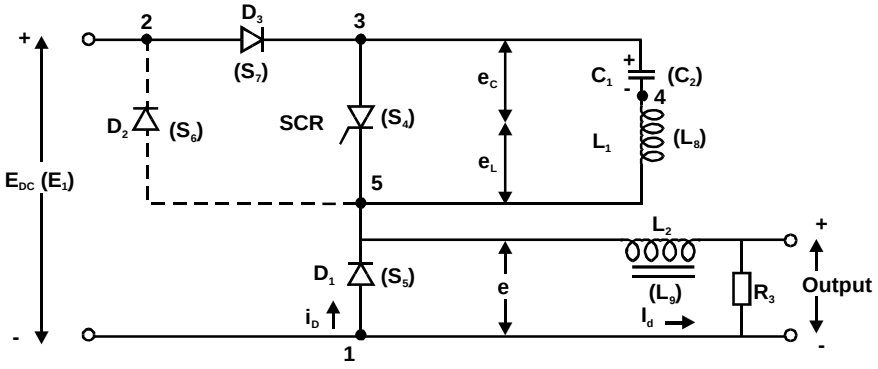

Fig. 1: An oscillating chopper

The graph of the chopper is obtained as shown in Fig. 2. The reactive elements are C_2, L_8 and L_9, which give the possible state variables as v_2, i_8 and i_9 [8, 9].

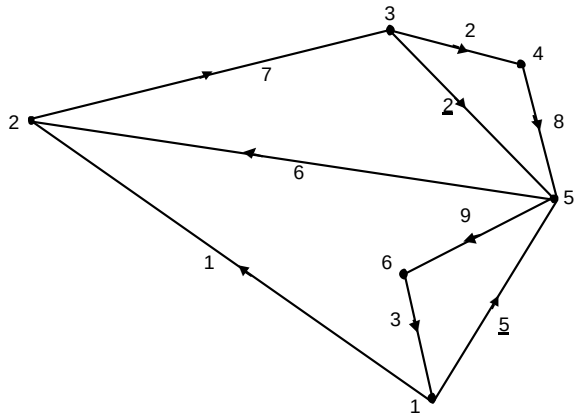

Fig. 2: Graph of the oscillating chopper

From Fig. 2, the complete incidence matrix is obtained as:

$$\beta_a = \begin{array}{c|ccccccccc} \text{nodes} & \multicolumn{9}{c}{\text{branches}} \\ & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 \\ \hline 1 & 1 & 0 & -1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 2 & -1 & 0 & 0 & 0 & 0 & -1 & 1 & 0 & 0 \\ 3 & 0 & 1 & 0 & 1 & 0 & 0 & -1 & 0 & 0 \\ 4 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 5 & 0 & 0 & 0 & -1 & -1 & 1 & 0 & -1 & 1 \\ 6 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & -1 \end{array} \quad (2)$$

ALGORITHM FOR OBTAINING THE MODIFIED COMPLETE INCIDENCE MATRIX

1. Replace the non-zero entries in the columns of β_A corresponding to the off-switches by zeroes;
2. If there exists a row where one non-zero entry occurs, replace the non-zero entry by a zero;
3. Repeat step 2. for columns;
4. Repeat steps 2. and 3. till none of the rows and columns contain one non-zero entry;
5. Formulate the modified complete incidence matrix, β_{AM}, by removing the rows and columns containing all zeroes.

APPLIYING THE ALGORITHM

In a situation where the switch branches 4, 5 and 7 in Fig. 2 are 'off', they are removed from the graph and, therefore, have no to and fro nodes. The non-zero entries in the columns representing the branches 4, 5 and 7 of β_A are, therefore, changed to zero ones by assigning θ to them. This is shown in equation 3.

$\beta_a =$

nodes \ branches	1	2	3	4	5	6	7	8	9
1	1	0	-1	0	θ	0	0	0	0
2	-1	0	0	0	0	-1	θ	0	0
3	0	1θ	0	θ	0	0	θ	0	0
4	0	-1θ	0	0	0	0	0	1θ	0
5	0	0	0	θ	θ	1	0	-1θ	1
6	0	0	1	0	0	0	0	0	-1

(3)

From equation (3), it is observed that row 3 has only one non-zero entry. Node 3, therefore, becomes a hanging node and is removed by changing the non-zero entry to zero. As can be seen, this does not apply to other rows since they contain more than one non-zero entries. The removal of the hanging node 3 is felt on branch 2 because there exists only one non-zero entry in column 2. Therefore, branch 2 is removed. Hanging node 4 and hanging branch 8 are also removed from the graph; all redundant columns and rows are removed (see Fig. 3). Hence, the modified incidence matrix, β_{AM}, for the stated switching device conditions is given by equation (4).

$\beta_{am} =$

nodes \ branches	1	3	6	9
1	1	-1	0	0
2	-1	0	-1	0
5	0	0	1	1
6	0	1	0	-1

(4)

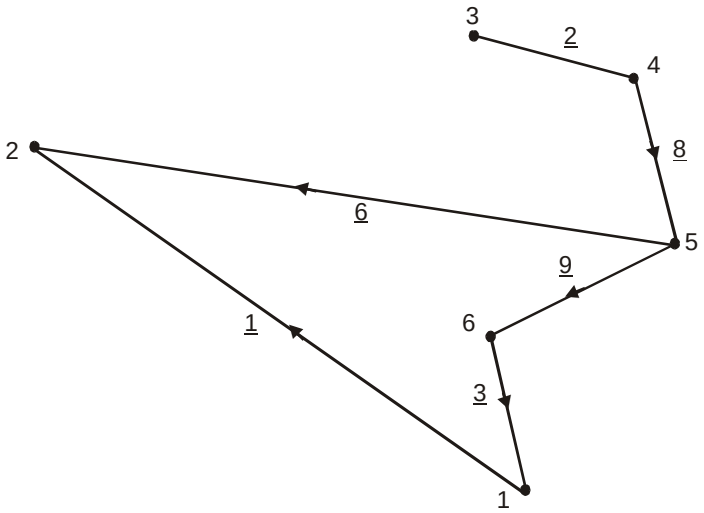

Fig. 3: Hanging nodes and branches of the graph

NORMAL TREE

Taking node 1 as the datum node, the incidence matrix becomes:

$$\beta_{am} = \begin{array}{c|cccc} \textbf{nodes} & \textbf{branches} & & & \\ & 1 & 3 & 6 & 9 \\ \hline 2 & -1 & 0 & -1 & 0 \\ 5 & 0 & 0 & 1 & 1 \\ 6 & 0 & 1 & 0 & -1 \end{array} \tag{5}$$

To construct the normal tree, branches 1, 3 and 6 represent the tree branches while branch 9 represents the link branch. Thus,

$$\alpha = [\alpha_T \mid \alpha_L] \tag{6}$$

where,

$$\alpha_T = \begin{bmatrix} -1 & 0 & -1 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix} \tag{7}$$

and

$$\alpha_L = \begin{bmatrix} 0 \\ 1 \\ -1 \end{bmatrix} \tag{8}$$

Therefore, the normal tree corresponding to off-switch branches of the chopper is shown in Fig. 4.

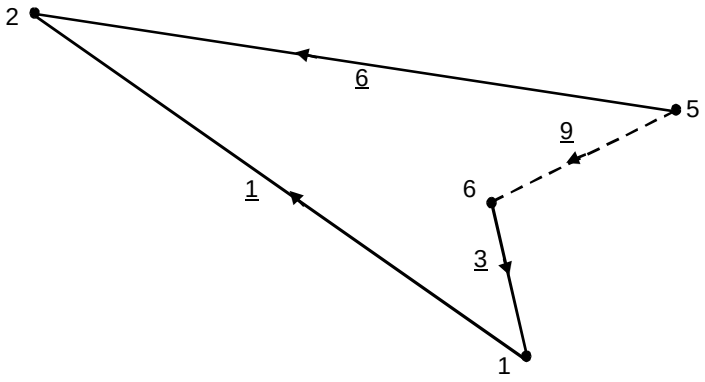

Fig. 4: Normal tree

FORMULATION OF STATE EQUATIONS USING SIGNAL-FLOW GRAPH

Signal flow is a natural concept that can be used in analysing the behaviour of a system. The signal-flow graph is a representation of a system in a topological form that features the interconnective aspects of the system [8]. The graph was developed with a more uniform notation than the block diagram and with a graphical representation that is more convenient to draw and easier to visualise.

SIGNAL-FLOW GRAPH FOR THE CHOPPER

Assuming the current distribution as shown by the direction of the arrowheads of Fig. 4, application of Kirchoff's voltage and current laws, respectively give:

$$E_1 - v_6 + v_9 + v_3 = 0 \quad (9)$$

$$i_1 = i_6 = i_9 = i_3 \quad (10)$$

Equation (9) can be re-written in terms of the circuit elements as:

$$E_1 - iR_6 + L_9\frac{di}{dt} + iR_3 = 0 \quad (11)$$

Taking the Laplace transform of equation (11) and re-arranging gives:

$$\frac{I(s)}{E_1(s)} = \frac{1}{R_6 - R_3 - L_9 s} \quad (12)$$

The signal-flow graph corresponding to equation (12) is shown in Fig. 5.

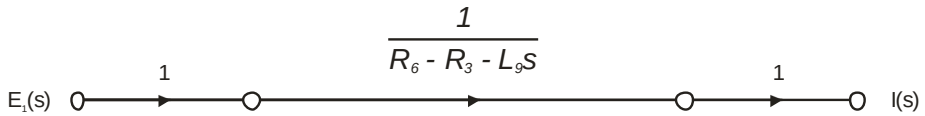

Fig. 5: Signal-flow graph

Recall that the state variables in the chopper circuit are v_2, i_8 and i_9. The signal-flow graph of Fig. 5 does not reflect the state variable in inductor L_9. The state variable is the current in L_9, which will be denoted by:

$$x_3 = i_9 \quad (13)$$

where,

$$v_9 = 9\frac{ds_3}{dt} = 9\bar{x}_3 \quad (14)$$

Note that s ≡ d/dt. Similarly, the state variables for C_2 and i_8 are:

$$x_1 = v_2 \tag{15}$$

and

$$x_2 = i_8 \tag{16}$$

where,

$$i_2 = 2\frac{dv_2}{dt} = 2\dot{x}_1 \tag{17}$$

and

$$v_8 = 8\frac{di_s}{dt} = 8\dot{x}_2 \tag{18}$$

In order to incorporate the state variable in inductor L_9, we re-write equations (9) and (10), respectively, as:

$$v_9 = -E_1 - v_3 + v_6 \tag{19}$$

$$i_6 = i_9;\ i_3 = i_9 \tag{20}$$

The signal-flow graph corresponding to equations (19) and (20) is shown in Fig. 6.

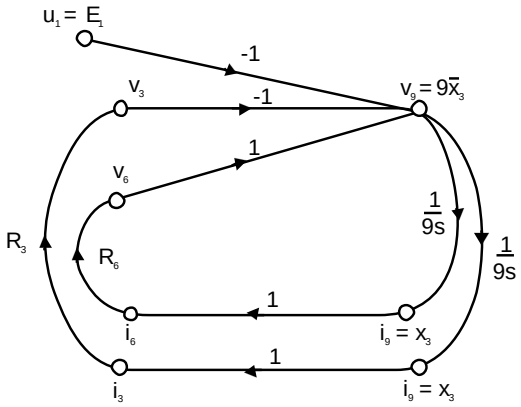

Fig. 6: Signal-flow graph with state variable in L_9

This graph is reduced by Mason's Rule [8, 9] to find the transmittances. One of these transmittances (1/9s) is already known from the original graph. The transmittance from $u_1 = E_1$ to $9x_3$ is:

$$\frac{9\dot{x}_3}{u_1} = \frac{-1(1)}{1} = -1 \tag{21}$$

Similarly,

$$\frac{9\dot{x}_3}{x_3} = \frac{R_6(1+0) - R_3(1+0)}{1} = R_6 - R_3 \tag{22}$$

From these transmittances, therefore, the reduced graph is shown in Fig. 7.

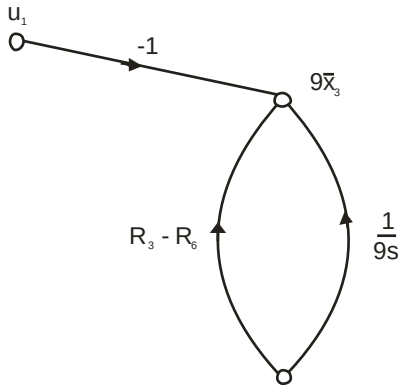

Fig. 7: Reduced signal-flow graph

STATE EQUATIONS AND SOLUTION

The state equation normally takes the form:

$$\frac{dx}{dt} = A_1 x + B_1 u \tag{23}$$

where, x is the state vector, u, the input vector and the matrices A_1 and B_1 are obtainable from the reduced signal-flow graph of Fig. 7. It is possible to evaluate the matrices on the basis of cut-set sub-matrix, Q_1 [7], where,

$$Q_1 = \alpha_T^{-1} \alpha_L \tag{24}$$

Since the topological method is used, the state equation corresponding to the graph of Fig. 7 is obtained directly as:

$$9(sx_3) = (R_6 - R_3)x_3 - u_1 \tag{25}$$

Equation (25) may be re-written as:

$$(sx_3) = \frac{1}{9}(R_6 - R_3)x_3 - \frac{1}{9}u_1 \tag{26}$$

This can now be written, in terms of derivatives, as:

$$\frac{d}{dt}\begin{bmatrix} \\ \cdots \\ i_9 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ \cdots & \cdots & \cdots \\ 0 & 0 & (R_6 - R_3) \end{bmatrix}\begin{bmatrix} \\ \cdots \\ i_9 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \cdots \\ -1/9 \end{bmatrix} u_1 \tag{27}$$

Alternatively,

$$\frac{d}{dt}\begin{bmatrix} \\ i_9 \end{bmatrix} = \begin{bmatrix} \\ 1/L_9 \end{bmatrix}\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & (R_6 - R_3 \end{bmatrix}\begin{bmatrix} \\ i_9 \end{bmatrix} + \begin{bmatrix} \\ 1/L_9 \end{bmatrix}\begin{bmatrix} 0 \\ 0 \\ -1/9 \end{bmatrix}\begin{bmatrix} E_1 \\ \end{bmatrix} \tag{28}$$

As branches 2 and 8 are removed from the graph of Fig. 3, the state variables v_2 and i_8 and the derivatives di_8/dt and dv_2/dt are forced to zero. By using the network topology, therefore, the state equation is given by:

$$\begin{bmatrix}1 & 1 & -1 & \cdots & 1\end{bmatrix}\begin{bmatrix}v_1\\ v_3\\ v_6\\ \cdots\\ v_9\end{bmatrix} = 0 \tag{29}$$

The general form is:

$$[\alpha]v = \begin{bmatrix}\alpha_T & \cdots & \alpha_L\end{bmatrix}\begin{bmatrix}v_T\\ \cdots\\ v_L\end{bmatrix} = 0 \tag{30}$$

Observe that we have one equation containing one unknown since $u_1 = E_1$ and $i_9 = i_1$ are known source voltage and current, respectively. The equation is, therefore, solvable. By referring to the reduced graph of Fig. 7 and applying Mason's Rule, the branch voltages v_3 and v_6 can be obtained.

Hence,

$$v_3 = \left[\frac{R_3(1)}{(1-0)}\right]x_3 = R_3 x_3 \tag{31}$$

Similarly,

$$v_6 = \left[\frac{R_6(1)}{(1-0)}\right]x_3 = R_6 x_3 \tag{32}$$

Alternatively,

$$\begin{bmatrix}v_3\\ v_6\end{bmatrix} = \begin{bmatrix}0 & 0 & R_3\\ 0 & 0 & R_6\end{bmatrix}x_3 \tag{33}$$

The result obtained can be verified by substituting equations (33) and (13) into equation (27) to give the Kirchoff's voltage equation (9).

Suppose the off-switch branches were not considered, the state equation would be given by:

$$\begin{bmatrix}
1 & 0 & 1 & 0 & 0 & -1 & 0 & \cdots & 0 & 1\\
1 & 0 & 0 & 0 & -1 & -1 & 0 & \cdots & 0 & 0\\
0 & 0 & -1 & 0 & -1 & 0 & 0 & \cdots & 0 & -1\\
0 & 0 & 0 & 1 & 0 & 1 & 1 & \cdots & 0 & 0\\
0 & 1 & 0 & 0 & 0 & 1 & 1 & \cdots & 1 & 0\\
0 & 1 & 0 & -1 & 0 & 0 & 0 & \cdots & 1 & 0\\
1 & 0 & 1 & 1 & 0 & 0 & 1 & \cdots & 0 & 1\\
0 & 0 & 0 & 1 & 0 & 1 & 1 & \cdots & 0 & 0\\
1 & 1 & 0 & 0 & -1 & 0 & 1 & \cdots & 1 & 0
\end{bmatrix}\begin{bmatrix}v_1\\ v_2\\ v_3\\ v_4\\ v_5\\ v_6\\ v_7\\ v_8\\ v_9\end{bmatrix} = \begin{bmatrix}0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\end{bmatrix} \tag{34}$$

It is worth pointing out that if any device in the circuit turns on or off, another corresponding normal tree will have to be constructed from the complete incidence matrix, β_A, and the state equations would, again, be formulated.

CONCLUSION

The complete incidence matrix has been developed and modified for a thyristor circuit – the chopper. Its normal tree and corresponding signal-flow graph were developed, the transmittance of which produces the reduced graph. From the reduced graph, the state equations were formulated and their solution obtained. The open-circuit conditions of branches 2 and 8 forced the derivatives of their state variables to zero.

A similar work utilised the normal form of the state equations to formulate the state equations in analysing a chopper [6] whereas the present work derives the state equations directly from the signal-flow graph. Although observing similar results which are in agreement with each other, the present approach, being purely topological, provides better possibility of computerising the analysis. The present approach, therefore, has the advantage of providing minimal computation time.

Conclusively, therefore, removing the open-circuit branches eliminates the problem of varying time constants in the solution of the state equations in the thyristor circuits.

REFERENCES

1. Ramamoorty, M. (1977). An introduction to thyristors and their applications. Affiliated East-West Press, pp. 4-5;
2. Niyi, Ogundana (2007): Fundamental principles of power electronics, Labari Communication, Nigeria, pp. 42;
3. Humphrey, A. J. (1996): Inverter commutation circuits, IEEE/IGA conference, October 1996, pp. 97-108;
4. Sen, P. C. (1992). Power electronics. 5th Edition, Tata McGraw Hill, pp. 849;
5. Murakami, Y., Kosaka, N., Nishimura, M. and Sakuma, N. (1971). Simulation program for thyristor circuits and its applications. Electrical Engineering, Japan, Vol. 91, pp. 51-59;
6. Revankar, G. N. Topological approach to thyristor-circuit analysis. Proceedings of the Institution of Electrical Engineering, United Kingdom, Vol. 120, No. 11, pp.1403-1405;
7. Revankar, G. N. and Mahajan, S. A. (1973). Digital simulation for mode identification in thyristor circuits. Proceedings of the Institution of Electrical Engineering, United Kingdom, Vol. 120, No. 2, pp.269-272;
8. Lago, G. V. and Benningfield, L. M. (1979). Circuit and system theory. John Wiley, New York, pp. 471-483; 553-554;
9. Adegboye, B. A. (2000). Oscillating chopper analysis using network topology. Spectrum Journal, Nigeria, Vol. 7, No. 2, pp. 23-33.